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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,470	03/29/2001	Yoshihiro Yoneda	82-01	5656

7590 12/04/2002

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EXAMINER

PATEL, ISHWARBHAI B

ART UNIT PAPER NUMBER

2827

DATE MAILED: 12/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/931,250	TAKAHASHI ET AL <i>[Signature]</i>
	Examiner	Art Unit
	Cassandra Cox	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) Responsive to communication(s) filed on 20 September 2002 .

2a) This action is **FINAL**.                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) 13-15 is/are allowed.

6) Claim(s) 1-5,10-12,16-20 and 22 is/are rejected.

7) Claim(s) 6-9,21,23 and 24 is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 17 August 2001 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some \* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_ .
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ .
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .	6) <input type="checkbox"/> Other: _____ .

## **DETAILED ACTION**

### ***Information Disclosure Statement***

The examiner has not considered the Information Disclosure Sheet referred to by the applicant in the amendment filed August 12, 2002 because there does not appear to be a copy of the IDS form 1449. The examiner requests that applicant submits a copy of the form 1449, so that the examiner may consider any relevant art.

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Objections***

2. The claims are objected to because they include reference characters which are not enclosed within parentheses.

Reference characters corresponding to elements recited in the detailed description of the drawings and used in conjunction with the recitation of the same element or group of elements in the claims should be enclosed within parentheses so as to avoid confusion with other numbers or characters which may appear in the claims. See MPEP § 608.01(m).

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in–  
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the

treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or  
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 1-5, 10-12, 16-20, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamauchi et al. (U.S. Patent No. 6,472,917).

In reference to claim 1, Yamauchi discloses in Figures 3 and 6 an integrated circuit comprising a driver circuit (600), a first long-distance wiring connected to the driver circuit (600), and a plurality of gate circuits (200, see Figure 6 also) connected over the entire length of the first long-distance wiring, so that an input signal (CK) is received by the plurality of gate circuits (200) via the driver circuit (600) connected to an end of the first long-distance wiring and an input terminal of the driver circuit (600) are connected through a second long distance wiring and a speed increasing circuit (800, 1200 in Figure 6). The same applies to claim 16.

In reference to claim 2, Yamauchi discloses in Figure 3 that the speed-increasing circuit (800) includes a PMOS transistor (301, 801, 802). The same applies to claim 17.

In reference to claim 3, Yamauchi also discloses in Figure 3 that the speed-increasing circuit (800) includes an NMOS transistor (302) and a buffer circuit (700) that is inserted at an input side of the second long-distance wiring. The same applies to claims 10, 18 and 22.

In reference to claim 4, Yamauchi discloses in Figure 3 that the speed-increasing circuit (800) includes a CMOS inverter having a PMOS transistor (301) and an NMOS transistor (302). The same applies to claims 11 and 19.

In reference to claim 5, Yamauchi discloses in Figure 6 a plurality of speed-increasing circuits (1200) additionally inserted between an intermediate position of the second long-distance wiring and the vicinity of the input terminal of the gate circuit (200) connected to that intermediate position. The same applies to claims 12 and 20.

***Allowable Subject Matter***

5. Claims 13-15 are allowed.

The following is an examiner's statement of reasons for allowance: Claim 13 is allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 5 wherein a plurality of buffer circuits (200, 201) are inserted at the input side of the second long-distance wiring (106) in combination with the rest of the limitations of the base claim and any intervening claims.

Claim 14 is allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 6 wherein a buffer circuit (201) is inserted at the output side of the second long-distance wiring (106) in combination with the rest of the limitations of the base claim and any intervening claims.

Claim 15 is allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 9 wherein the gate circuits (203) are realized by flip-flop circuits in combination with the rest of the limitations of the base claim and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. Claims 6-9, 21, and 23-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Claims 6 and 21 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 5 wherein a plurality of buffer circuits (200, 201) are inserted at the input side of the second long-distance wiring (106) in combination with the rest of the limitations of the base claim and any intervening claims.

Claim 7 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 6 wherein a buffer circuit (201) is inserted at the output side of the second long-distance wiring (106) in combination with the rest of the limitations of the base claim and any intervening claims.

Claims 8 and 23 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 7 wherein the input signal (VIN) is realized by a word line selecting signal; the driver circuit (100) is realized by a word line driver; the first long-distance wiring (104) is realized by a word line; and the gate circuits (103) are realized by memory cells in combination with the rest of the limitations of the base claims and any intervening claims.

Claims 9 and 24 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 9 wherein the gate circuits (203) are realized by

flip-flop circuits in combination with the rest of the limitations of the base claim and any intervening claims.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 703-306-5735. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703)-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

CC  
CC  
December 1, 2002

*Keane B. Lee*  
Keane B. Lee  
Patent Examiner  
Art Unit 2816